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Name: U.S. Patent & Trademark Office
FAX: (703) 872-9306
Application No.: 10/602,357
Filing Date: June 23, 2003
Inventor: BENWARE, Robert
Art Unit: 2857
Examiner: Raymond, Edward
From: Eric J. Whitesell, Reg. No. 38,657 *EW*
Today's Date: November 1, 2004
Attorney Docket No.: 02-6301 81563/6653
Pages: 12 pages (including this 1-page coversheet)
Dispatched by: Susan R. Telford

Transmitted herewith for filing via facsimile:

Transmittal Form (1 pg.); Amendment "A" (10 pgs.); Fax coversheet (1 pg.)

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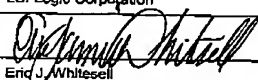
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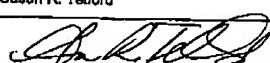
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Transmittal Form (to be used for all correspondence after initial filing)	Application Number	10/602,357
	Filing Date	6/23/2003
	First Named Inventor	BENWARE, Robert
	Art Unit	2857
	Examiner Name	Raymond, Edward
Total Number of Pages in This Submission		12
Attorney Docket Number		02-6301 81583/8853

ENCLOSURES (CHECK ALL THAT APPLY)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm name	LSI Logic Corporation		
Signature			
Printed Name	Eric J. Whitesell		
Date	November 1, 2004	Reg No.	38,657

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Amendment "A" page 1 of 10
10/602,357

DOCKET NO. 02-6301
81563 (6653)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): BENWARE, Robert
Serial No.: 10/602,357
Filed: June 23, 2003
For: METHOD OF SCREENING
DEFECTS USING LOW VOLTAGE
IDDQ MEASUREMENTS
Art Unit: 2857
Examiner: Raymond, Edward

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November 1, 2004

Susan R. Telford

AMENDMENT "A" UNDER 37 C.F.R. § 1.111

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